COLLEGE OF NATURAL AND COMPUTATIONAL SCIENCE

DEPARTMENT OF PHYSICS

GROUP PRESENTATION OF PHYSICS OF ELECTRONICS (II)

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1. Metal-Oxide Semiconductor (MOS) Structure

A basic MOS consisting of three layers:

i) The top layer is a conductive metal electrode

The “metal” plate is a heavily doped p$^+$ - apoly-silicon layer which behaves as a metal.

ii) The middle layer is an insulator of glass or silicon dioxide,

The insulating layer is silicon dioxide and the other plate of the capacitor is the semiconductor layer which in our case is n-type silicon whose resistivity is 1-10 Ω-cm corresponding to a doping of 10^{15} cm^{-3}.

iii) The bottom layer is another conductive electrode made out of crystal silicon

This layer is a semiconductor whose conductivity changes with either doping or temperature.

Cross-section of a MOS diode, d is the thickness of the oxide and V is the applied voltage on the metal field plate, V> (<) 0 metal plate is positively (negatively) biased with respect to the ohmic contact.

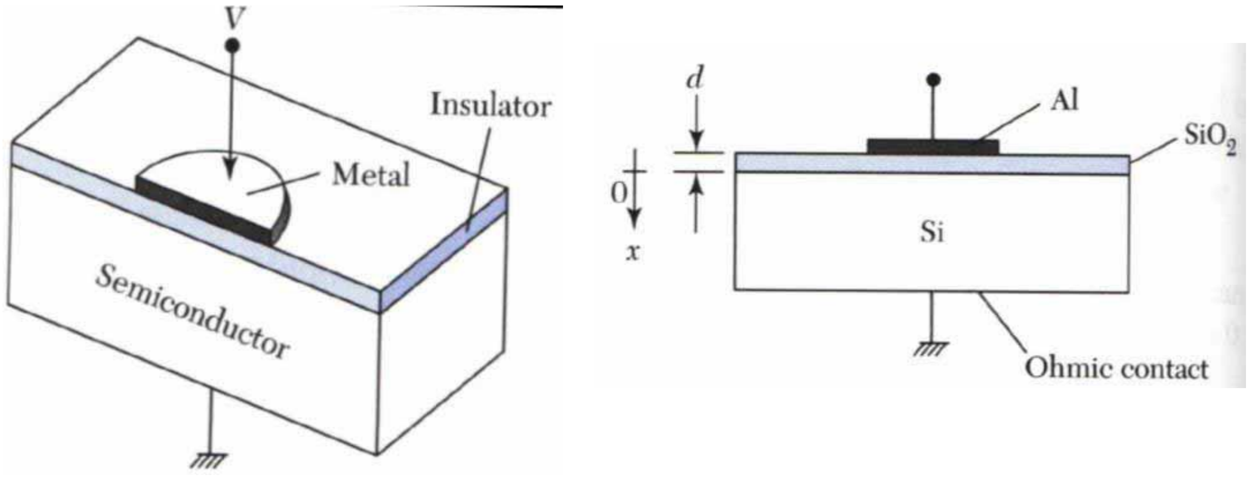


Figure 1: The MOS structure of layers

The capacitance of the MOS structure depends on the voltage (bias) on the gate. For the purposes of this discussion, we shall refer to the contact to the semiconductor as the body (B) while the poly-silicon is called the gate (G). Typically a voltage is applied to the gate while the body is grounded and the applied voltage is V_G but more accurately V_{GB}. The two (V_G & V_{GB}) will be used interchangeably in this document.

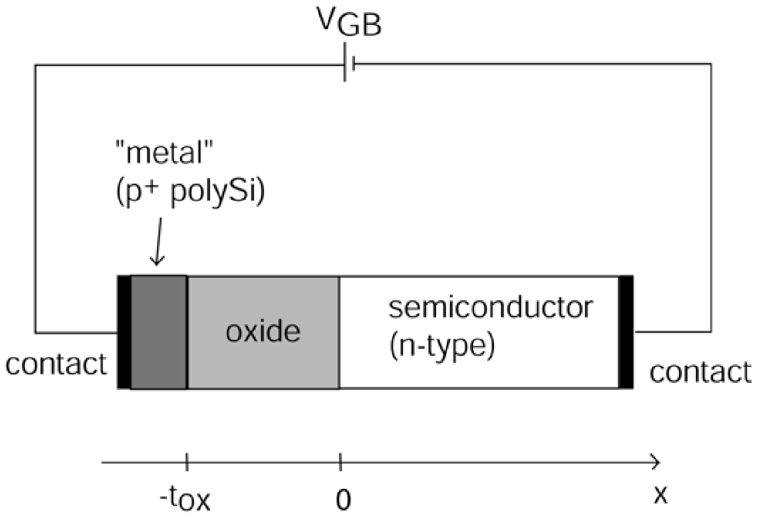
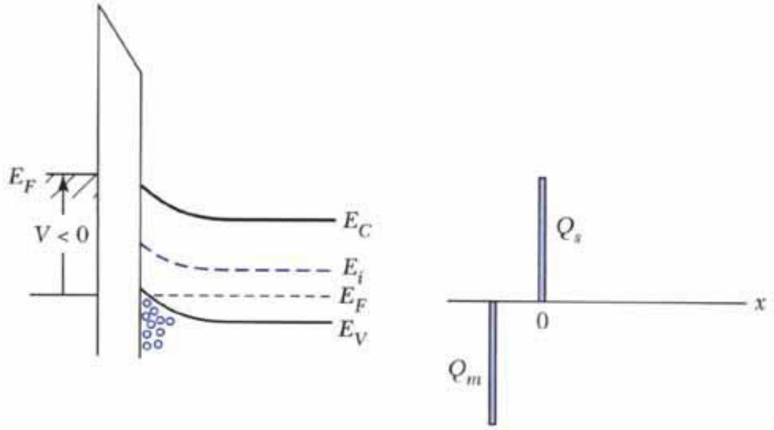


Figure 2: The MOS Capacitor structure. The substrate (body) is grounded and a voltage V_{GB} is applied to the poly-silicon gate.

When an ideal MOS diode is biased with positive or negative voltages, three cases may exist at the semiconductor surface.

A. accumulation
B. depletion
C. inversion

A. Accumulation

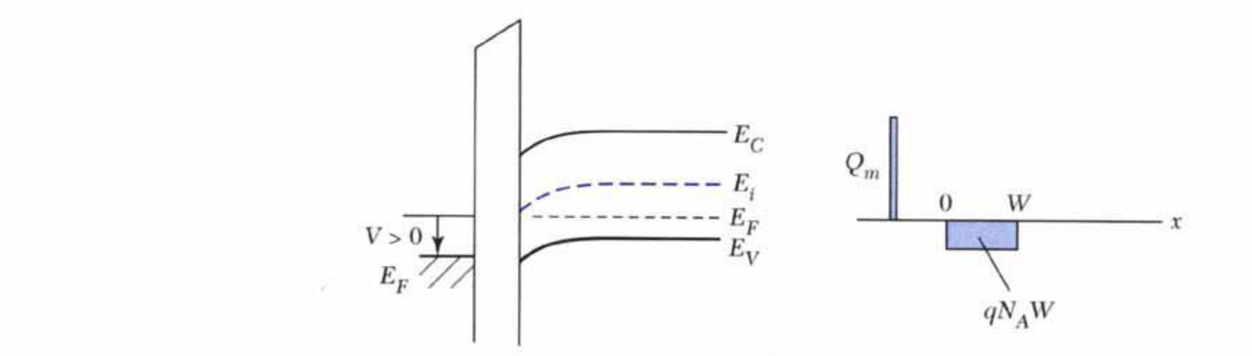


- $V<0$
- excess ”+” carrier will be induced at the SiO2-Si interface
- Bands near the semiconductor surface are bent upward

$$p_p = n_i e^{(E_i - E_F)/kT} . \quad (1)$$

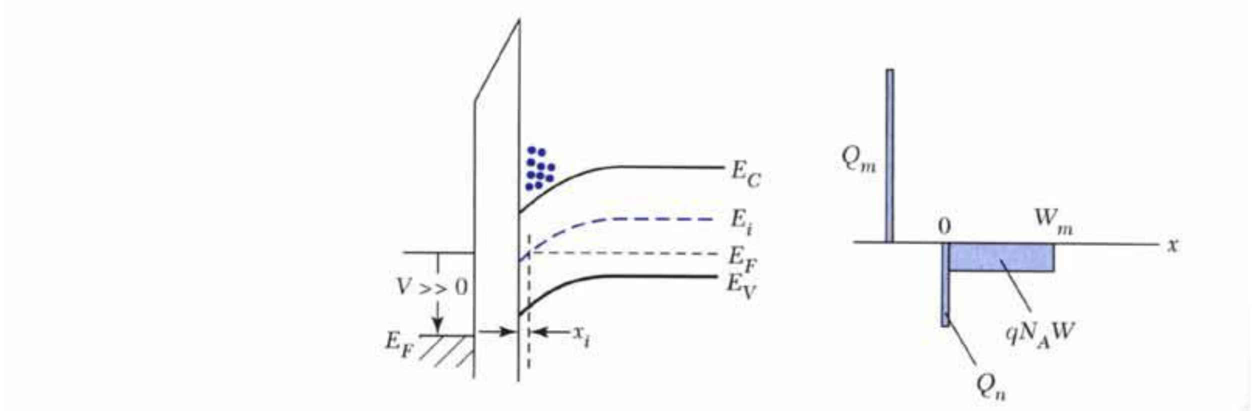
- Charge distribution Qs=lQml (Qs + charge per unit area in the semiconductor)

B. Depletion



- V>0
- Bands near the semiconductor surface are bent downward and the major carriers (holes) are depleted
- Charge distribution $Qsc = -qNAW$ (space charge per unit area) W (width of depletion region)

C. Inversion



- Larger +V is applied →E_i cross over the Fermi level

$$n_p = n_i e^{(E_F - E_i)/kT} . \tag{2}$$

- Electrons is greater than holes
- Weak and strong inversion (electron concentration in interface equal to the substrate doping level)
- After this point additional e in the n-type inversion layer(1~10nm)

$$Q_s = Q_n + Q_{sc} = Q_n - qN_AW_m , \tag{3}$$

2. Power metal – oxide semiconductor FET (MOSFET)

Power MOSFET is a specific type of MOSFET designed to handle large amounts of power and it is the majority carrier devices, so they perform better in high frequency applications where switching power losses are important.

Power MOSFETs can withstand of high current and voltage without undergoing destructive failure due to second breakdown (BJT case), are based on isolated gate, that makes it easy to drive with minimum of power requirement and main advantages are high commutation speed, superior switching speed and good efficiency at low voltages.

Power MOSFET's major drawback is on-resistance RDS (on) and its strong positive temperature coefficient. At high breakdown voltages (>200V) the on-state voltage drop of the power MOSFET becomes higher Power MOSFET is the most widely used as a low-voltage (i.e. less than 200V) switch mode power-supply (SMPS) converter applications.

It can be found in most power supplies, DC to DC converters, and low voltage motor controllers.

2.1. Power MOSFET: Lateral v/s Vertical Structure

Power MOSFETs have a vertical structure compared to ordinary MOSFET having Lateral structure. D-MOSFET can be built using either a Lateral or vertical structure. In a lateral structure (ordinary MOSFET), current & breakdown voltage ratings are both functions of the channel dimensions (respectively width & length of the channel), resulting in inefficient use of the "silicon estate". Lateral structure is more suitable for integration and provides lower capacitance and higher speed. With a vertical structure (Power MOSFETs), voltage rating is function of the doping and thickness of the N-epitaxial layer, while current rating is a function of the channel width. This makes possible device able to sustain both high blocking voltage and high current within a compact piece of silicon. The vertical structure supports higher breakdown voltage, lower on-resistance and higher current capability.

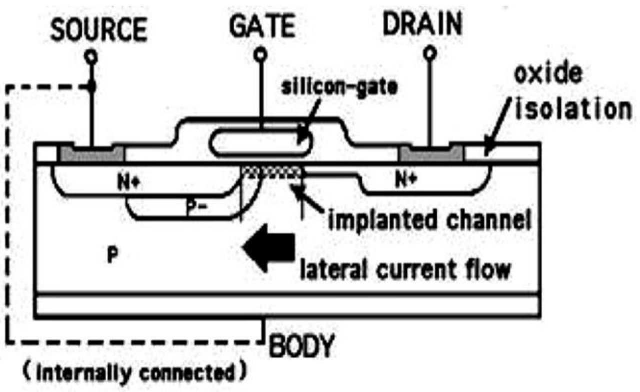


Figure1a. Lateral Structure

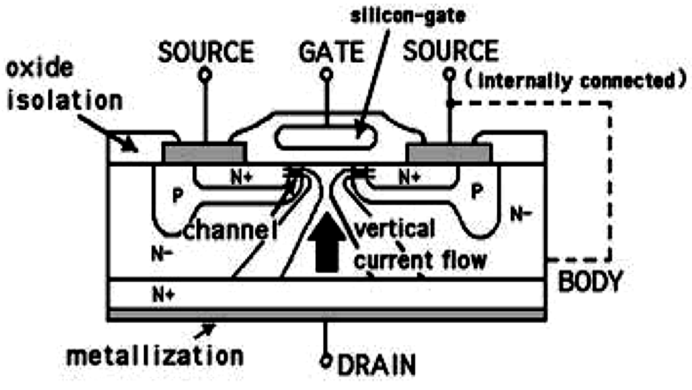


figure1b.Vertical Structure

2.2. Power MOSFET: Intrinsic body diode & Parasitic BJT

Power MOSFET has a parasitic BJT as an integral part of its structure. The body region serves as the base, source as the emitter and the drain as the collector. It is important to keep this BJT OFF of all times by keeping the potential of the base as close to the emitter potential as possible. This is accomplished by shorting the body and the source part of the MOSFET. Otherwise, the potential at the base would turn on the BJT and lead the device into the “latch up” condition, which would destroy the device.

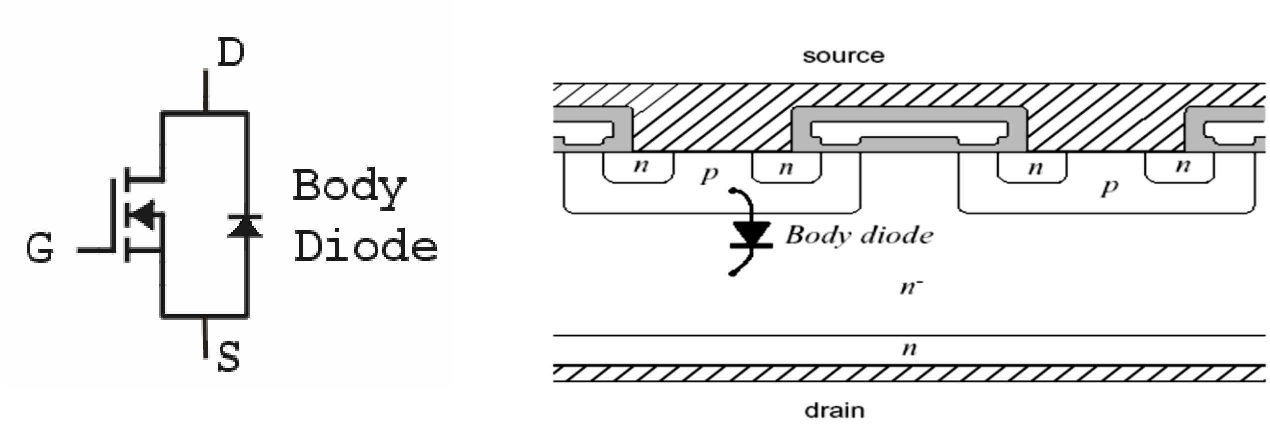


Figure2. Intrinsic body diode

3. Metal-Semiconductor contact

When a metal and semiconductor are brought into contact, there are two types of junctions formed depending on the work function of the semiconductor and its relation with the metal.

1. Schottky junction - $\phi_M > \phi_{semi}$
2. Ohmic junction - $\phi_M < \phi_{semi}$

3.1. Schottky junction

Consider a junction formed between a metal and n-type semiconductor, as shown in figure 3. The Fermi level of the semiconductor is higher (since its work function is lower) than the metal. Similar to a metal-metal junction, when the metal-semiconductor junction is formed the Fermi levels must line up at equilibrium. Another way to look at this is that there are electrons in the conduction level of the semiconductor which can move to the empty energy states above the Fermi level of the metal. This leave a positive charge on the semiconductor side and due to the excess electrons, a negative charge on the metal side, shown in figure 4, leading to a contact potential . When a contact is formed between two metals, the charges reside on the surface. This is due to the high electron density found in metals (typically10^{22}cm ^{3}). On the other hand, when a contact is formed between a metal and semiconductor, due to the low charge density on the semiconductor side (typically 10^{17} cm^3) the electrons are removed not only from the surface

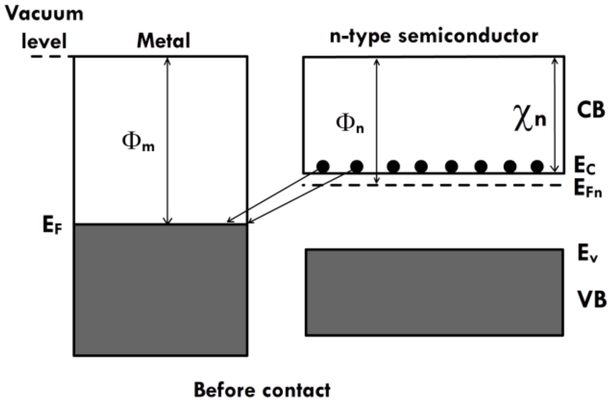


Figure 3: Schottky junction between metal and n-type semiconductor before contact.

The work function of the semiconductor is smaller than the metal so that electrons can move from semiconductor to metal, forming a contact potential.

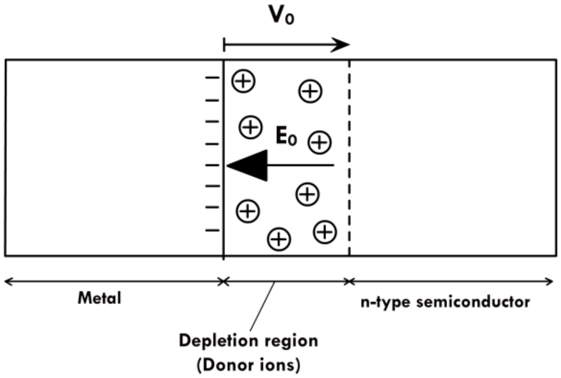


Figure 4: Schematic showing the metal, n-type semiconductor, and the Schottky junction between them. There is a depletion layer in the n-type semiconductor due to transfer of electrons to the metal. This leads to the formation of a contact potential.

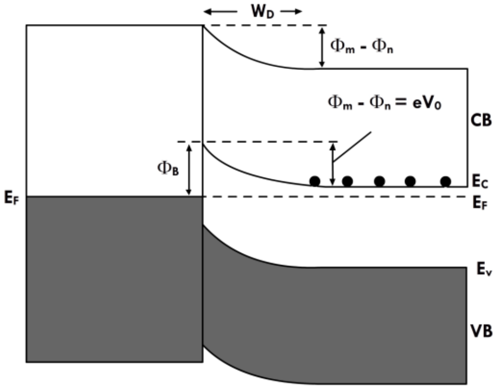


Figure 5: Schottky junction showing the band bending on the semiconductor side. Semiconductor bands bend up going from the semiconductor (positive) to metal (negative) since this is the same direction as the electric field, but also from a certain depth within the semiconductor. This leads to the formation of a depletion region within the semiconductor, shown in figure 4. Thus, when a Schottky junction is formed between the metal and semiconductor, the Fermi level lines up and also a positive potential is formed on the semiconductor side. Because the depletion region extends within a certain depth in the semiconductor there is bending of the energy bands on the semiconductor side. Bands bend up in the direction of the electric field (field goes from positive charge to negative charge, opposite of the potential direction). This means the energy bands bend up going from n-type semiconductor to metal, shown in figure 5. The Fermi levels line up and there is a certain region in the semiconductor (denoted by W) where the bands bend (this is the depletion region). Another name for the depletion region is the space charge layer. There is a built in potential in the Schottky junction, V0, and from figure 5 this is given by the difference in work functions.

$$eV_0 = \phi_M - \phi_{semi} \tag{4}$$

The work function of the metal is a constant while the semiconductor work function depends on the doping concentration (since this affects the Fermi level position). The contact potential then represents the barrier for the electrons to move from the n-type semiconductor to the metal. Initially, when the junction is formed electrons move to the metal to create the depletion region. The contact potential thus formed prevents further motion of the electrons to the metal. There is also a barrier for electrons to move from metal to semiconductor. This is called the Schottky barrier and denoted by ϕ_B in figure 5. This is given by

$$\phi_B = (\phi_m - \phi_n) + \left(E_c - E_{F_c}\right) = \phi_m - \chi_n \tag{5}$$

Where χ_n is the electron affinity of the n-type semiconductor?

At equilibrium the motion of electrons from the semiconductor to metal is balanced by the contact potential so that there is no net current. The Schottky junction can be biased by application of an external potential.

There are two types of bias

1. Forward bias - metal is connected to positive terminal and n-type semi- conductor connected to negative terminal
2. Reverse bias - metal is connected to negative terminal and n-type semiconductor connected to positive terminal. The current flow depends on the type of bias and the amount of applied external potential.

3.1.1. Forward bias

In a forward biased Schottky junction the external potential is applied in such a way that it opposes the in-built potential. Since the region with the highest resistivity is the depletion region near the junction, the voltage drop is across the depletion region. Under external bias the Fermi levels no longer line up, but are shifted with respect to one another and the magnitude of the shift depends on the applied voltage. Energy band diagram of the Schottky junction under forward bias is shown in figure 6. Thus, electrons injected from the external circuit into the n-type semiconductor have a lower barrier to surmount before reaching the metal. This leads to a current in the circuit which increases with increasing external potential. The current in a Schottky diode under forward bias is given by

$$J = J_0\left[\exp\left(\frac{eV}{K_B T}\right) - 1\right] \tag{6}$$

Where J is the current density for an applied potential of V_0, J_0 is a constant and depends on the Schottky barrier (ϕ_B) for the system and the expression
is

$$J_0 = AT^2 \exp\left(-\frac{\phi_B}{K_B T}\right) \tag{7}$$

Where A is the Richardson constant for thermionic emission and is a material property. Equation 3 shows that in the forward bias the current exponentially increases with applied potential.

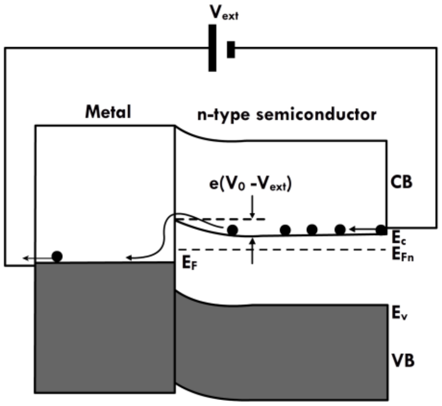


Figure 7: Schottky junction under forward bias.

3.1.2. Reverse bias

In the case of a reverse bias the external potential is applied in the same direction as the junction potential, as shown in figure 8. Once again the Fermi levels no longer line up but the barrier for electron motion from the n-type semiconductor to metal becomes higher. The electron flow is now from the metal to the semiconductor and the barrier for this is given by the Schottky barrier(ϕ_B). So there is a constant current in reverse bias, whose magnitude is equal to J_0 (as given in equation 4). From calculations it can be shown that the current in the forward bias is orders of magnitude higher than the current in reverse bias (this arises due to the exponential dependence on potential). So a Schottky junction acts as a rectifier i.e. it conducts in forward bias but not in reverse bias.

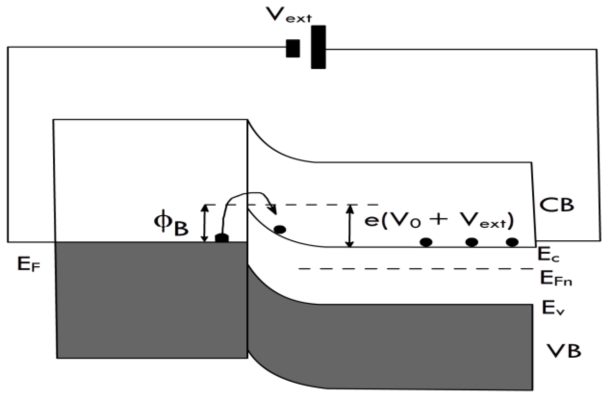


Figure 8: Schottky junction under reverse bias.

The forward and reverse bias currents for a Schottky junction formed between Si and Au can be calculated using equations 3 and 4. The doping concentration fixes the Fermi level position in the semiconductor and hence its work functions. Using equation 4 it is possible to calculate the reverse saturation current density in this junction. The forward bias current density depends on the applied voltage, equation 3, and increases exponentially with the applied voltage

3.2. Ohmic Junction

A Schottky junction is formed when the semiconductor has a lower work function than the metal. When the semiconductor has a higher work function the junction formed is called the Ohmic junction. Once again it is possible to draw the energy band diagram of the junction in equilibrium (Fermi levels line up). This is shown in figure 13. At equilibrium, electrons move from the metal to the empty states in the conduction band so that there is an accumulation region near the interface (on the semiconductor side). The accumulation region has a higher conductivity than the bulk of the semiconductor due to this higher concentration of electrons. Thus, a Ohmic junction behaves as a resistor conducting in both forward and reverse bias. The resistivity is determined by the bulk resistivity of the semiconductor.

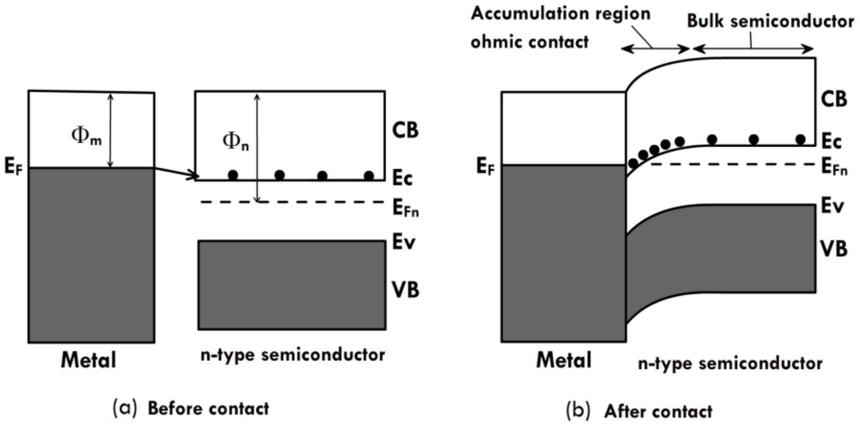


Figure 9: Ohmic junction (a) before and (b) after contact.

Before contacts the Fermi levels are at different positions and they line up on contact to give an accumulation region in the semiconductor.

4. Metal-semiconductor Field-effect Transistor (MESFET)

The Metal-Semiconductor-Field-Effect-Transistor (MESFET) consists of a conducting channel positioned between a source and drain contact region. The carrier flow from source to drain is controlled by a Schottky metal gate. The control of the channel is obtained by varying the depletion layer width underneath the metal contact which modulates the thickness of the conducting channel and thereby the current between source and drain. The key advantage of the MESFET is the higher mobility of the carriers in the channel as compared to the MOSFET. Since the carriers located in the inversion layer of a MOSFET have a wave function, which extends into the oxide, their mobility - also referred to as surface mobility is less than half of the mobility of bulk material. As the depletion region separates the carriers from the surface their mobility is close to that of bulk material. The higher mobility leads to a higher current, transconductance and transit frequency of the device.

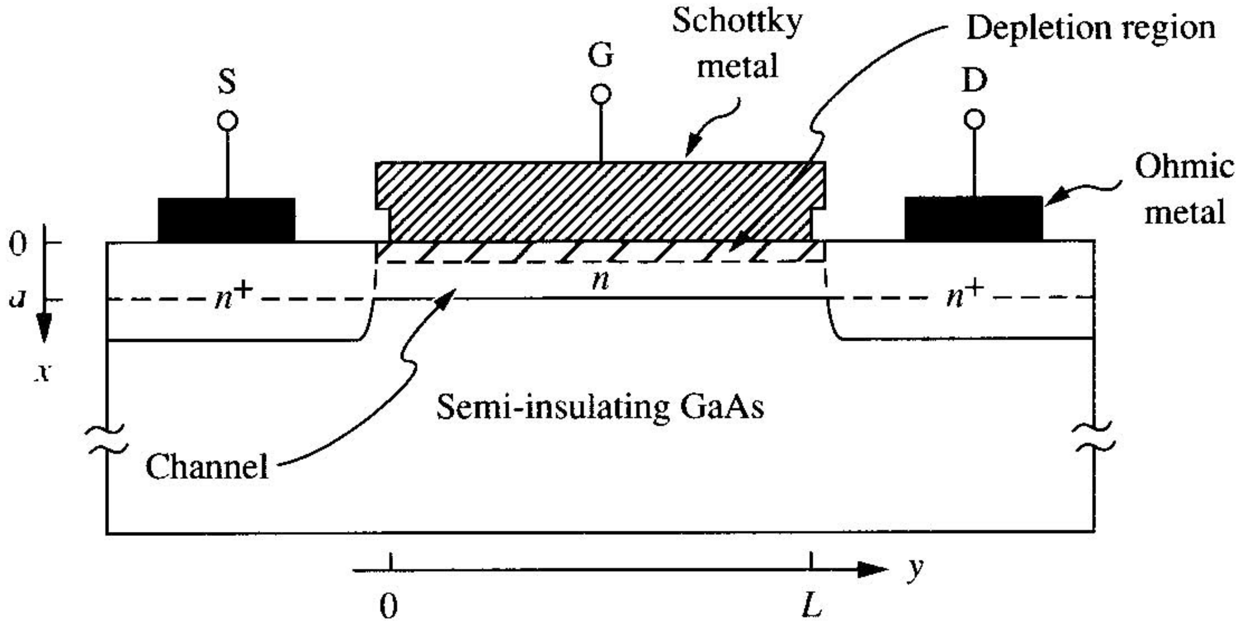
The disadvantage of the MESFET structure is the presence of the Schottky metal gate. It limits the forward bias voltage on the gate to the turn-on voltage of the Schottky diode. This turn-on voltage is typically 0.7 V for GaAs Schottky diodes. The threshold voltage therefore must be lower than this turn-on voltage. As a result it is more difficult to fabricate circuits containing a large number of enhancement-mode MESFET.

The use of GaAs rather than silicon MESFETs provides two more significant advantages: first, the electron mobility at room temperature is more than 5 times larger, while the peak electron velocity is about twice that of silicon. Second, it is possible to fabricate semi-insulating (SI) GaAs substrates, which eliminates the problem of absorbing microwave power in the substrate due to free carrier absorption.

If the MOS junction is replaced by a direct metal-semiconductor contact, i.e., a Schottky barrier, it is called metal-semiconductor FET (MESFET).

A MESFET is similar to a JFET except for the following differences:

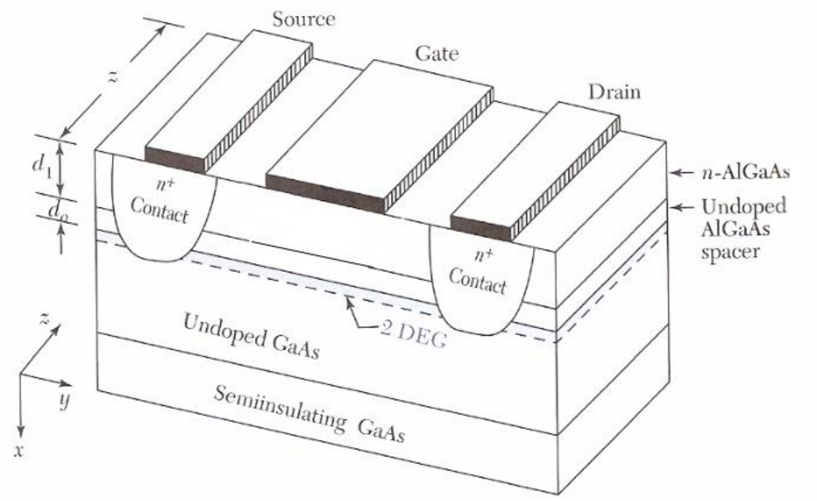
- **(i)** It has a single gate
- **(ii)** The gate is formed by a metal-semiconductor junction



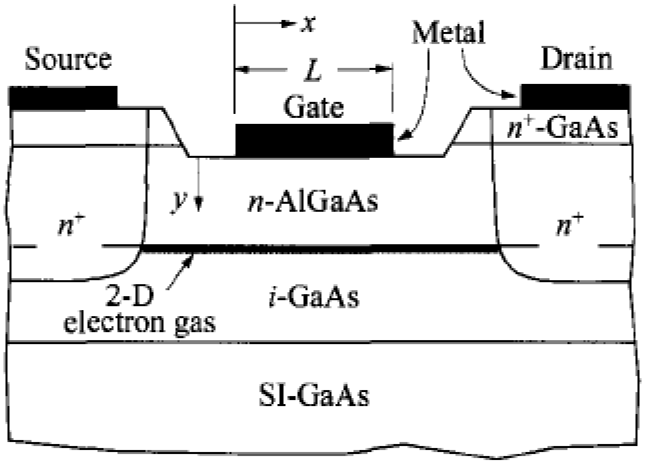
The operation is very similar to that of a JFET. The p-n junction gate is replaced by a Schottky barrier, and the lower contact and p-n junction are eliminated because the lightly doped p type substrate is replaced by a semi-insulating substrate.

5. Modulated-doped field-effect transistor (MODFET)

MODFET are similar to MESFET, but with the difference that MODFET's are made of different kind of semiconductors (heterojunction). The two different semiconductors create at the interface a very good conductive channel (2DEG). The mobility of the electrons in this channel is very high, which is one of the reasons they are very fast. To deplete the channel a negative voltage must be applied at the gate. The voltage you need to deplete the channel is called the threshold voltage.



- Modulated-doped field-effect transistor (also known as HEMT (high-electron mobility transistor))



- Heterostructure: wide band gap material is doped and carriers diffuse to the undoped, narrow band gap layer at which hetero interface the channel is formed.
- Channel carriers in the un doped hetero interface are spatially separated from the doped region and have high motilities because there is no impurity scattering.
- The main advantage of modulation doping is the superior mobility. (no scattering)

Basic device structure of MODFET:

The principle of modulation doping is:

- Carriers from the doped barrier layer are transferred to reside at the heterointerface and are away from the doped region to avoid impurity scattering.

- AlGaAs/GaAs hetero interface: barrier layer AlGaAs under the gate is doped and channel layer GaAs is undoped.

A hetero junction is a junction between two semiconductors with a different band gap. In case of a MODFET the channel is un doped to avoid scattering at impurities. The n doping is made a bit away from the channel, but the donors still contribute electrons to the conduction band. At the junction the bands bend and because of the differed band gaps the conduction band gets bend below the Fermi energy and creates a low density metal. The idea is to use this metal as the conductive channel. The advantage is that it's possible to deplete the channel with the gate and that the channel has a very high mobility.

MODFET's can be found in high frequency preamplifier like in cell phones, electronic warfare systems, microwave and millimeter wave communications, radar, and radio astronomy. They are very fast and can be used at frequencies up to 600 GHz and more. They also have a high gain and low noise.

Summary

Power MOSFET is a specific type of MOSFET designed to handle large amounts of power and it is the majority carrier devices, so they perform better in high frequency applications where switching power losses are important. Power MOSFETs have a vertical structure compared to ordinary MOSFET having Lateral structure. Lateral structure is more suitable for integration and provides lower capacitance and higher speed. The vertical structure supports higher breakdown voltage, lower on-resistance and higher current capability. Power MOSFET has a parasitic BJT as an integral part of its structure. The body region serves as the base, source as the emitter and the drain as the collector.

When a metal and semiconductor are brought into contact, there are two types of junctions formed depending on the work function of the semiconductor and its relation with the metal. The work function of the semiconductor is smaller than the metal so that electrons can move from semiconductor to metal, forming a contact potential.

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